Docket No.: SL-081

Harrington & Smith, LLP Docket No.: 907.0018.USU

Patent Application Papers of: Leroy A. Gibson Jr., Dan M. Griffin, Lyman D. Horne, Randal R. Sylvester

Method and Device for Frame Sync Detection Using Channel Combining and Correlation

Method and Device for Frame Sync Detection Using Channel Combining and Correlation

BACKGROUND

1. Field of Use

These teachings relate generally to communications systems such as wireless data or telephone systems. More particularly, the invention relates frame sync detection using channel combining and correlation in systems requiring frame synchronization.

2. Description of Prior Art

A variety of multiple access communication systems have been developed for transferring information among a large number of system users. Techniques employed by such multiple access communication systems include time division multiple access (TDMA), frequency division multiple access (FDMA), and AM modulation schemes, such as amplitude companded single sideband (ACSSB), the basics of which are well known in the art.

In Spread Spectrum (SS) or TDMA-SS transmission systems a succession of short-duration bursts emanating from a number of different stations are presented to a demodulator. Each burst may contain data frames from one or more data channels. Each data frame generally contains a synchronization or sync word and a data payload area. The sync word must be rapidly identified in order to continue processing the data through subsequent processes such as de-interleaving or forward error correction (FEC) control circuits. Consequently rapid-identification of the sync word and its position within the stream of data is desired.

In general, identification of a sync word is accomplished by transmitting the sync word at a higher power level. The higher the power levels the higher the probability of finding the sync

word. However, it can be readily appreciated that higher power levels used to transmit sync words lead to other disadvantages such as cross channel interference, or a difficulty in controlling the automatic gain control (AGC) circuits of the transmitter and the receiver. For example, higher power levels for sync words can cause reception problems in satellite systems where the power levels across multiple signals must have approximately equal signal strength. This is particularly necessary if Intermediate Frequency (IF) limiting or traveling wave tube amplifiers are employed in order to avoid suppression of weaker signals. In addition, systems relying on a high power sync word or frame may never achieve synchronization if the energy level of the sync word is degraded during transmission.

Another method for achieving frame sync is to find frame sync in consecutive frames. Each time the frame sync is found a confidence counter is incremented. Once the counter reaches a predetermined level then synchronization is declared. However, this approach requires the reception of multiple frames, as well as having to look for each phase ambiguity in systems where phase ambiguity is an issue. This procedure is also time intensive.

Therefore, it is desirable to reduce the amount of power required for frame sync. It is also desirable to provide rapid identification of frame sync even though frame sync power is decreased either through design or path degradation. It is further desirable to make more efficient use of the energy being transferred into the various communication channels or signals within a communication system.

SUMMARY OF THE PREFERRED EMBODIMENTS

The foregoing and other problems are overcome, and other advantages are realized, in accordance with the presently preferred embodiments of these teachings. As will be described below, important aspects of the invention reside in the summing of sync words from more than one channel in order to achieve frame sync.

In accordance with one embodiment of the invention a method for frame sync detection using signal combining and correlation is provided. The method includes the steps of despreading PN coded signals to provide in-phase I_1-I_n, and quadrature phase Q_1-Q_n signals, wherein each I_1-I_n and each Q_1-Q_n signal contains at least one sync bit, and where $n \geq 2$. The at least one sync bit from each of the I_1-I_n and quadrature phase Q_1-Q_n signals are summed to form sums I_{s1} and Q_{s1}, respectively. The next step provides a reference sync having at least one bit and compares each sum I_{s1} and Q_{s1} with the at least one reference bit. The results of each I_{s1} and Q_{s1} comparison are accumulated so as to form two accumulates, I_A and Q_A, respectively. Each accumulate I_A and Q_A is squared to form I_A^2 and Q_A^2 from which the sum I_A^2 and Q_A^2 is formed. The sum $I_A^2 + Q_A^2$ is compared with a predetermined threshold and as a result of the comparison a determination of whether frame sync has been achieved is made.

In accordance with another embodiment of the invention a device for frame sync detection using channel combining and correlation is provided. The device includes a channel despreader, wherein the channel despreader provides at least two each in-phase I1-In and quadrature phase Q1-Qn channels, where $n \geq 2$. The device also

includes an I-sync processor and a Q-sync processor, both coupled to the channel despreader. The device also includes an address controller coupled to the I-sync processor and the Q-sync processor. A first summer connected to the I-sync processor and the Q-sync processor couples the sum to a threshold comparator for determination of sync detection.

Another embodiment of the invention is directed towards an integrated circuit (IC). The IC includes a channel despreader, providing at least two each in-phase I1-In and quadrature phase Q1-Qn channels, where n ≥ 2. The IC also includes at least one I-sync processor coupled to the channel despreader and at least one Q-sync processor, also coupled to the despreader. An on-board IC first summer is connected to the I-sync processor and the Q-sync processor from which a sum is coupled to an on-board IC sync detection comparator.

The invention is also directed towards a program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for frame sync detection using signal combining and correlation. The method includes the steps of despreading PN coded signals to provide in-phase I_1-I_n and quadrature phase Q_1-Q_n signals, wherein each I_1-I_n and each Q_1-Q_n signal contains at least one sync bit, and where $n \geq 2$. The at least one sync bit from each I_1-I_n, and quadrature phase Q_1-Q_n signals are summed to form sums I_{s1} and Q_{s1}, respectively. The next step provides a reference sync having at least one bit and compares each sum I_{s1} and Q_{s1} with the at least one reference bit. The results of each I_{s1} and Q_{s1} comparison are accumulated so as to form two accumulates, I_A and Q_A respectively. Each accumulate I_A and Q_A, is squared to form I_A^2 and Q_A^2 from which the sum I_A^2 and Q_A^2 is formed. The sum $I_A^2 + Q_A^2$ is compared with a predetermined threshold and as a result of the

comparison a determination of whether frame sync has been achieved is made.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects of these teachings are made more evident in the following Detailed Description of the Preferred Embodiments, when read in conjunction with the attached Drawing Figures, wherein:

Fig. 1 is block diagram of a terminal device and a base station connected to a wireless local area network incorporating features of the present invention;

Fig. 2 is a block diagram of the frame sync detector shown in Fig. 1; and

Fig. 3 is a flow chart of one method for frame sync detection for the system shown in Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although the present invention will be described with reference to the embodiment shown in the drawings, it should be understood that the present invention could be embodied in many alternate forms of embodiments. Exemplary, but not limiting embodiments include: mobile telephone systems requiring the reception and/or transmission of data and/or a satellite data system where information in the form of data is transmitted to a user.

Referring now to Fig. 1 there is shown an illustration for a wireless user terminal 10, such as but not limited to wireless

local area networks (LANs) 17 that are suitable for practicing this invention. The wireless user terminal 10 includes an antenna 12 for transmitting signals to and for receiving signals from a base site 13, as well as a base transceiver station 14. In the preferred embodiment the transmitted signals are code division multiple access (CDMA) signals.

The mobile station and base transceiver station 14 includes a modulator (MOD) 14A, a transmitter 14, a receiver 16, a frame sync detector 20, and a controller 18 that provides signals to and receives signals from the transmitter 14 and receiver 16, respectively. It should be understood that the terminal device 10 could be vehicle mounted or a stationary device.

Referring also to Fig. 2 there is shown a block diagram of the frame sync detector 15 incorporating features of the present invention. It is understood that the signals received and despread by despreader 21 may have been transmitted by any suitable transmission technique in which a pseudo-noise (PN) code is employed as a modulation waveform. Exemplary, but not limiting, modulation techniques include direct sequence spread spectrum (DSSS) or Frequency Hop Spread Spectrum (FHSS) systems.

Referring also to Fig. 3, Despreader 21 de-spreads 31, 31A a received signal by multiplying a signal modulated by the spreading code sequence (PN) of a received signal and a replica of the spreading code sequence (PN) at the receiving end, thereby taking a correlation between the two code sequences. Then, the correlation output is detected, and the establishment of the signal synchronization is detected by testing whether or not the detection output exceeds a threshold. If the signal synchronization has not yet been established, the phase of the replica of the spreading code sequence is shifted, and the detection of the synchronization is tested again. This is

performed until the signal synchronization is established. The output of the despreader 21 is an I_{1-n} and Q_{1-n} digital data stream.

The I_{1-n} and Q_{1-n} data streams are parallel-clocked one bit at a time corresponding to a recovered symbol clock into column adders 22,22A, respectively. Adders 22,22A sum 32,32A the columns of bits and couples the sums to Dual Port RAMs 23, 23A. In the preferred embodiment the column sums are truncated to an eight-bit resolution. In alternate embodiments the sum resolution could be any suitable bit resolution.

Dual Port Rams 23,23A in the preferred embodiment are 16 x 16 dual port rams. In alternate embodiments the Dual Port Rams 23,23A could be any suitable matrix size. The added data is clocked into the Dual Port Rams 23,23A at the recovered symbol rate to an address controlled by address counter 24. The summed data representing the column sums are clocked out of the Dual Port RAMs 23,23A at a higher rate than the data is clocked in, preferably 32 or 64 times faster. The data is bit precision sign extended to 12 bits, or any suitable precision, and coupled to multipliers 25,25A where it is compared with known sync word 26, 33,33A. Converting the known sync word 26 to a series of 1's and/or -1's and then multiplying the converted sync word with the summed data accomplishes the comparison.

Registers 27,27A, adders 28,28A, and registers 29,29A accumulate the result of multipliers 25,25A, 34,34A. In the preferred embodiment registers 27,27A, 29,29A are D-Type latch registers or devices that perform similar functionality. In the preferred embodiment the result of multipliers 25,25A are accumulated a number of times equal to the length of the sync word 26. In alternate embodiments the number of accumulations could be any suitable number to determine sync.

The accumulated I values and Q are then coupled to squarers 210 and 210A and squared 35,35A, respectively, and subsequently summed 36 in adder 211 to provide non-coherent power detection. In the preferred embodiment squarer 210 is time shared so as to perform the functionality of squarer 210A. The sum of the squares is latched through register 212 to comparator 213 where it is compared 37 with a predetermined threshold. In an alternate embodiment the square root of the output of adder 211 could be taken in order to provide other system processing information.

If the summed columns from the I_{1-n} and Q_{1-n} data streams do not correspond to the sync word 26 then the accumulated value will be below a predetermined threshold and a no sync condition would be declared 39. Alternatively, if the summed columns from the I_{1-n} and Q_{1-n} data streams do correspond to the sync word 26 then the accumulated value will be relatively large and if the sum of the squares exceeds the predetermined threshold then comparator 213 outputs sync detect signal and frame sync is declared 30.

It should be understood that the foregoing description is only illustrative of the invention. Moreover, it will be readily appreciated that an advantage of the present invention is the use of multiple channels to detect frame sync. It will be further appreciated that advantages of the present invention include an effective increase of approximately 12 dB in the power level of the sync word (for a 16-bit sync word and twenty input channels I_1-I_{20} and Q_1 - Q_{20}). In addition, various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances that fall within the scope of the appended claims.